signetics

OBJECTIVE SPECIFICATION

BIPOLAR FIELD-PROGRAMMABLE LOGIC ARRAY (16X8X48 FPLA) 82S101 (OPEN COLLECTOR) 82S100 (TRI-STATE)

APRIL 1975

DIGITAL 8000 SERIES TTL/MEMORY

82S100
82S101

DESCRIPTION

The 82S100 (Tri-State Outputs) and the 82S101 (Open Collector Outputs) are Bipolar Programmable Logic Arrays, containing 48 Product terms (AND terms), and 8 output functions. Each output function can be programmed either true active-High (Fp), or true active-Low ($F\overline{p}$). The true state of the output functions is controlled via an output Sum (OR) Matrix by a logical combination of 16-input variables, or their complements, up to 48 terms.

Both devices are field-programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S100 and 82S101 are fully TTL compatible, and include a chip-enable clocking input for output deskewing and inhibit. They feature either Open Collector or Tri-State outputs for ease of expansion of product terms and/or input variables.

FEATURES

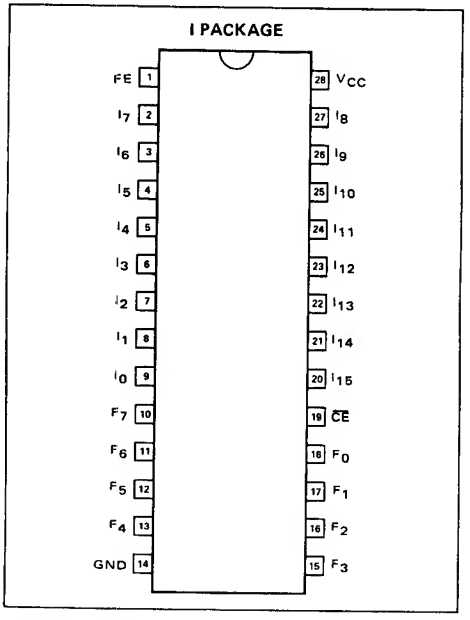
- FIELD PROGRAMMABLE (Ni-Cr LINK)
- INPUT VARIABLES – 16
- OUTPUT FUNCTIONS – 8
- PRODUCT TERMS – 48
- ADDRESS ACCESS TIME – 50ns, MAXIMUM
- POWER DISSIPATION – 600mW, TYPICAL
- INPUT LOADING – (–100μA), MAXIMUM
- OUTPUT OPTION:
  TRI-STATE OUTPUTS – 82S100
  OPEN COLLECTOR OUTPUTS – 82S101
- OUTPUT DISABLE FUNCTION:
  TRI-STATE – Hi-Z
  OPEN COLLECTOR – Hi
- CERAMIC DIP

APPLICATIONS

LARGE READ ONLY MEMORY
RANDOM LOGIC
CODE CONVERSION
PERIPHERAL CONTROLLERS
LOOK-UP AND DECISION TABLES
MICROPROGRAMMING
ADDRESS MAPPING
CHARACTER GENERATORS
SEQUENTIAL CONTROLLERS

PIN CONFIGURATION

I PACKAGE



TRUTH TABLE

LET:

$P_n = \prod_0^{15} (k_m I_m + j_m \overline{I_m})$; k = 0, 1, X (Don't Care)
n = 0, 1, 2, ... , 47

where:

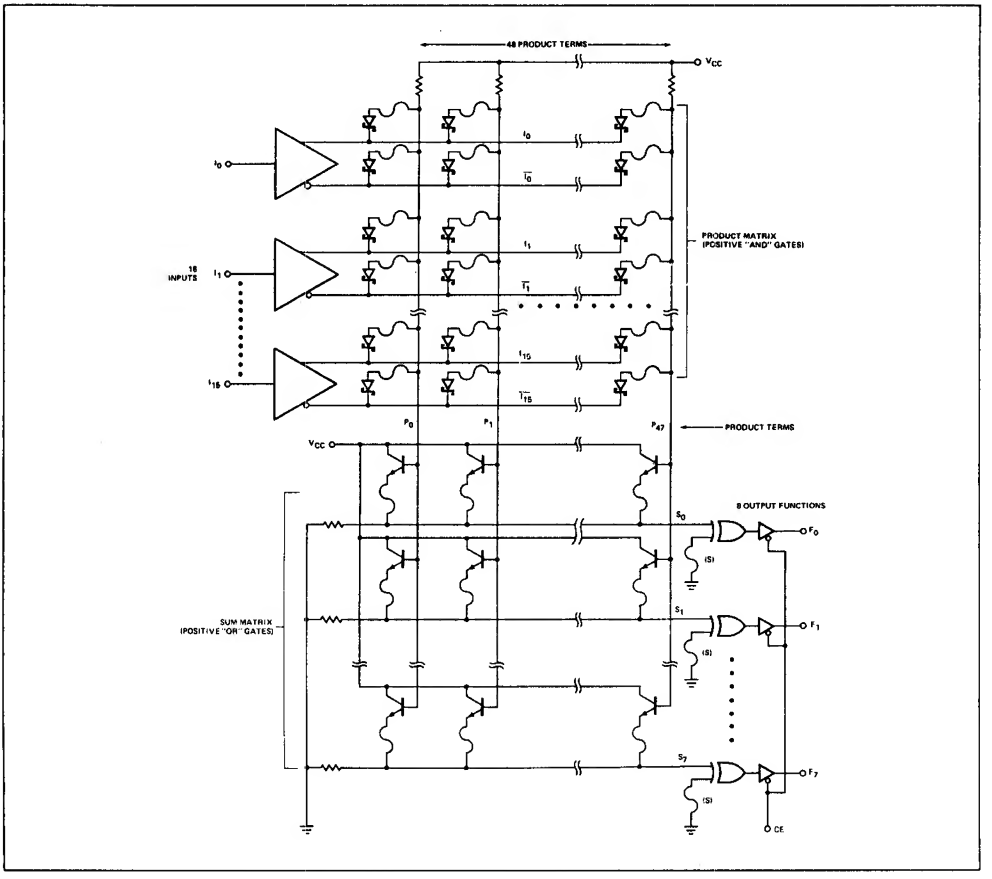
Unprogrammed state : $j_m = k_m = 0$

Programmed state : $j_m = \overline{k_m}$

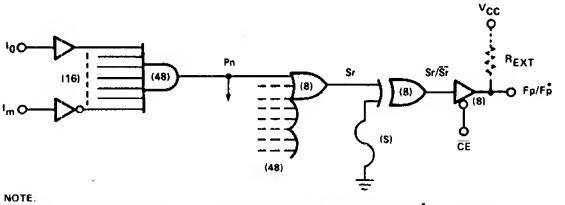
$S_r = f(\Sigma_0^{47} P_n)$; r ≡ p = 0, 1, 2, ... , 7

MODE	P_n	$\overline{CE}$	F_p	F_p^*	$S_r \stackrel{?}{=} f(P_n)$
Disabled (82S101)	X	1	1	1	X
Disabled (82S100)			Hi-Z	Hi-Z	
Read	1	0	1	0	YES
	0	0	0	1	
	X	0	0	1	NO

BLOCK DIAGRAM



FPLA TYPICAL LOGIC PATH



NOTE:
FOR EACH OF THE 8 OUTPUTS, EITHER THE FUNCTION Fp (ACTIVE HIGH) OR $\overline{Fp}$ (ACTIVE LOW) IS AVAILABLE, BUT NOT BOTH. THE REQUIRED FUNCTION POLARITY IS USER PROGRAMMABLE VIA FUSE (S).

$Pn = I_0 \cdot I_1 \cdot \overline{I_2} \cdot I_3 \cdot \ldots \cdot \overline{I_m}$

$Sr = P_0 + P_1 + P_2 + \ldots \ldots Pn$

$\overline{Sr} = \overline{P_0} \cdot \overline{P_1} \cdot \overline{P_2} \cdot \ldots \ldots \overline{Pn}$

$Fp = (\overline{CE}) + (Sr) = (\overline{CE}) + (P_0 + P_1 + P_2 + \ldots \ldots Pn)$ @ S = SHORT

$\overline{Fp} = (\overline{CE}) + (\overline{Sr}) = (\overline{CE}) + (\overline{P_0} \cdot \overline{P_1} \cdot \overline{P_2} \cdot \ldots \ldots \overline{Pn})$ @ S = OPEN

ABSOLUTE MAXIMUM RATINGS

PARAMETER[1]		RATING	UNIT
V_{CC}	Power Supply Voltage	+7	Vdc
V_{in}	Input Voltage	+5.5	Vdc
V_{OH}	High Level Output Voltage (82S101)	+5.5	Vdc
V_O	Off-State Output Voltage (82S100)	+5.5	Vdc
T_A	Operating Temperature Range	0° to +75°	°C
T_{stg}	Storage Temperature Range	−65° to +150°	°C

ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq 75°C$; $4.75V \leq V_{CC} \leq 5.25V$

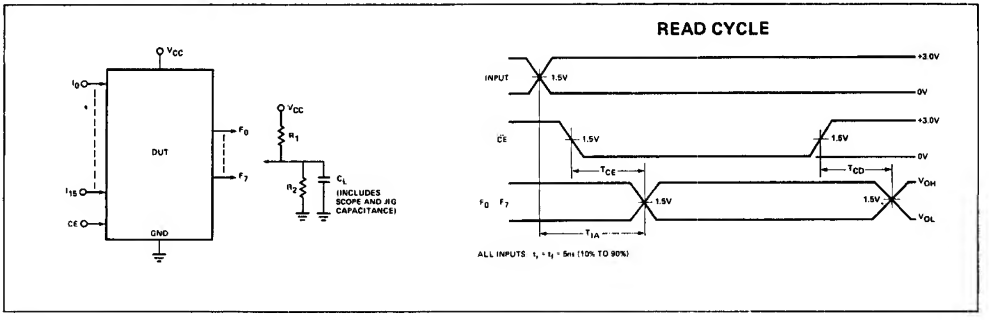
PARAMETER		TEST CONDITIONS		LIMITS MIN	LIMITS TYP[2]	LIMITS MAX	UNIT	NOTES
V_{IH}	High-Level Input Voltage	V_{CC} = 5.25V		2			V	1
V_{IL}	Low-Level Input Voltage	V_{CC} = 4.75V				0.8	V	1
V_{IC}	Input Clamp Voltage	V_{CC} = 4.75V, I_{IN} = −18mA			−0.8	−1.2	V	1, 7
V_{OH}	High-Level Output Voltage (82S100)	V_{CC} = 4.75V, I_{OH} = −2mA		2.4			V	1, 5
V_{OL}	Low-Level Output Voltage	V_{CC} = 4.75V, I_{OL} = 9.6mA			0.35	0.45	V	1, 8
I_{OLK}	Output Leakage Current (82S101)	V_{CC} = 5.25V	V_{OUT} = 5.25V		1	40	μA	6
$I_{O(OFF)}$	Hi-Z State Output Current (82S100)		V_{OUT} = 5.25V		1	40	μA	6
			V_{OUT} = 0.45V		−1	−40	μA	6
I_{IH}	High-Level Input Current	V_{IN} = 5.5V			<1	25	μA	
I_{IL}	Low-Level Input Current	V_{IN} = 0.45V			−10	−100	μA	
I_{OS}	Short-Circuit Output Current (82S100)	V_{CC} = 5.25V, V_{OUT} = 0V		−20		−70	mA	3, 7
I_{CC}	V_{CC} Supply Current (82S100, 82S101)	V_{CC} = 5.25V			120	170	mA	4
C_{IN}	Input Capacitance	V_{CC} = 5.0V	V_{IN} = 2.0V		5		pF	
C_O	Output Capacitance		V_{OUT} = 2.0V		8		pF	6

NOTES:
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Duration of short circuit should not exceed one second.
4. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic "1" stored.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Test each output one at the time.
8. Measured with a programmed logic condition for which the output under test is at a "0" logic level. Output sink current is supplied thru a resistor to V_{CC}.

SWITCHING CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[2]	MAX	
Propagation Delay						
T_{IA}	Input to Output	C_L = 30pF		35	50	ns
T_{CD}	Chip Disable to Output	R_1 = 270		15	20	ns
T_{CE}	Chip Enable to Output	R_2 = 600		15	20	ns

AC TEST FIGURE AND WAVEFORM



NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, and T_A = +25°C.

OBJECTIVE PROGRAMMING PROCEDURE

The 82S100/101 are shipped in an unprogrammed state, characterized by:

A. All internal Ni-Cr links are intact.

B. Each product term (P-term) contains both true and complement values of every input variable I_m (P-terms always logically "FALSE").

C. The Sum Matrix contains all 48 P-terms.

D. The polarity of each output is set to active HIGH (F_p function).

E. All outputs are at a LOW logic level.

To program each of 8 Boolean logic functions of 16 true or complement variables, including up to 48 P-terms, follow the Program/Verify procedures for the Product Matrix, Sum Matrix, and Output Polarity outlined below.

OUTPUT POLARITY

PROGRAM ACTIVE LOW (F_p^* Function)

Program output polarity before programming Product Matrix and Sum Matrix. Program one output at the time.

1. Set GND (pin 14) to OV.
2. Do not apply power to the device (V_{CC}, pin 28, open).
3. Apply V_{OUT} = +18V to the appropriate output for 1ms, and return to OV.
4. Repeat step 3 to program other outputs.

VERIFY OUTPUT POLARITY

1. Set GND (pin 14) to OV, and V_{CC} (pin 28) to +5V.
2. Enable the chip by setting $\overline{CE}$ (pin 19) to LOW logic level.
3. Disable input variables by applying V_{IN} = +10V to all inputs I_0 through I_{15}.
4. Verify output polarity by sensing the logic state of outputs F_0 through F_7. All outputs at a HIGH logic level are programmed active HIGH (F_p function), while all outputs at a LOW logic level are programmed active LOW (F_p^* function).
5. Remove V_{IN} = +10V from inputs I_0 through I_{15}.

PRODUCT MATRIX

PROGRAM INPUT VARIABLE

Program one input at the time and one P-term at the time. All input variable links of unused P-terms are not required to be fused. However, unused input variables must be programmed as Don't Care for all programmed P-terms.

1. Set GND (pin 14) to OV, and V_{CC} (pin 28) to +5V.
2. Disable the chip by setting $\overline{CE}$ (pin 19) to HIGH logic level.
3. Disable input variables by applying V_{IN} = +10V to all inputs I_0 through I_{15}.
4. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to

outputs F_0 through F_5 with F_0 as LSB. Use standard TTL logic levels.

5a. If the P-term contains neither I_0 nor $\overline{I_0}$ (input is a Don't Care), fuse both I_0 and $\overline{I_0}$ links by executing both steps 5b and 5c, before continuing with step 7.

5b. If the P-term contains I_0, set to fuse the $\overline{I_0}$ link by lowering the input voltage to I_0 from V_{IN} = +10V to a HIGH logic level. Execute step 6.

5c. If the P-term contains $\overline{I_0}$, set to fuse the I_0 link by lowering the input voltage to I_0 from V_{IN} = +10V to a LOW logic level. Execute step 6.

6a. After 10μs delay, raise FE (pin 1) from 0V to +17V. The source must have a current limit of 250mA, and rise time of 10 to 50μs.

6b. After 10μs delay, pulse the $\overline{CE}$ input to +10V for a period of 1ms.

6c. After 10μs delay, return FE input to 0V.

7. Return input I_0 to a disable state by applying V_{IN} = +10V.

8. Repeat steps 5 through 7 for all other input variables.

9. Repeat steps 4 through 8 for all other P-terms.

10. Remove V_{IN} = +10V from all input variables.

VERIFY INPUT VARIABLE

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +5V.

2. Enable F_7 output by setting $\overline{CE}$ to +10V.

3. Disable input variables by applying V_{IN} = +10V to inputs I_0 through I_{15}.

4. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to outputs F_0 through F_5.

5. Interrogate input variable I_0 as follows:
   A. Lower the input voltage to I_0 from V_{IN} = +10Vto a HIGH logic level, and sense the state of output F_7.
   B. Lower the input voltage to I_0 from a HIGH to a LOW logic level, and sense the logic state of output F_7.

The state of I_0 contained in the P-term is determined in accordance with the following truth table:

I_0	F_7	Input Variable State Contained In P-Term
0 1	1 0	$\overline{I_0}$
0 1	0 1	I_0
0 1	1 1	Dont Care
0 1	0 0	(I_0), ($\overline{I_0}$)

Note that two tests are required to uniquely determine the state of the input variable contained in the P-term.

6. Return input I_0 to a disable state by applying V_{IN} = +10V.

7. Repeat steps 5 and 6 for all other input variables.

8. Repeat steps 4 through 7 for all other P-terms.

9. Remove V_{IN} = +10V from all input variables.

SUM MATRIX

PROGRAM PRODUCT TERM

Program one output at the time for one P-term at the time. All P_n links of unused P-terms in the Sum Matrix are not required to be fused.

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +8.5V.

2. Disable the chip by setting $\overline{CE}$ (pin 19) to a HIGH logic level.

3. Address the P-term to be programmed (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5, with I_0 as LSB. Use standard TTL levels.

4a. If the P-term is contained in output function F_0 (F_0 = 1 or F_0^* = 0), go to step 6.

4b. If the P-term is not contained in output function F_0 (F_0 = 0 or F_0^* = 1), set to fuse the P_n link by applying V_{OUT} = +10V to output F_0.

5a. After 10μs delay, raise FE (pin 1) from 0V to +17V.

5b. After 10μs delay, pulse the $\overline{CE}$ input to +10V for a period of 1ms.

5c. After 10μs delay, return FE input to 0V.

6. Repeat steps 4 and 5 for all other output functions.

7. Repeat steps 3 through 6 for all other P-terms.

8. Remove +8.5V from V_{CC}.

VERIFY PRODUCT TERM

1. Set GND (pin 14) to 0V, and V_{CC} (pin 28) to +8.5V.

2. Enable the chip by setting $\overline{CE}$ (pin 19) to a LOW logic level.

3. Address the P-term to be verified (No. 0 through 47) by applying the corresponding binary code to input variables I_0 through I_5, with I_0 as the LSB. Use standard TTL levels.

4. To determine the status of the P_n link in the Sum Matrix for each output function F_p or F_p^*, sense the state of outputs F_0 through F_7. The status of the link is given by the following truth table:

Output		P-term Link
Active HIGH (F_p)	Active LOW (F_p^*)	
0	1	FUSED
1	0	PRESENT

5. Repeat steps 3 and 4 for all other P-terms.

6. Remove +8.5V from V_{CC}.

16 X 48 X 8 FPLA PROGRAM TABLE

THIS PORTION TO BE COMPLETED BY SIGNETICS

CF (XXXX) _____

CUSTOMER SYMBOLIZED PART # _____

DATE RECEIVED _____

COMMENTS _____

CUSTOMER NAME _____

PURCHASE ORDER # _____

SIGNETICS DEVICE # _____

TOTAL NUMBER OF PARTS _____

PROGRAM TABLE # _____ REV _____ DATE _____

PROGRAM TABLE ENTRIES

INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
I_m	T_m	DON'T CARE	PROD. TERM PRESENT IN F_p	PROD. TERM *NOT* PRESENT IN F_p	ACTIVE HIGH	ACTIVE LOW
H	L	X	A	–	H	L
NOTE: All unused inputs must be programmed as DON'T CARE			*NOTE: Output Function entries are independent of programmed output polarity*		*NOTE. Output Polarity Programmed once only*	

	PRODUCT TERM*																ACTIVE LEVEL							
	INPUT VARIABLE (I_m)																OUTPUT FUNCTION							
NO.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
0																								
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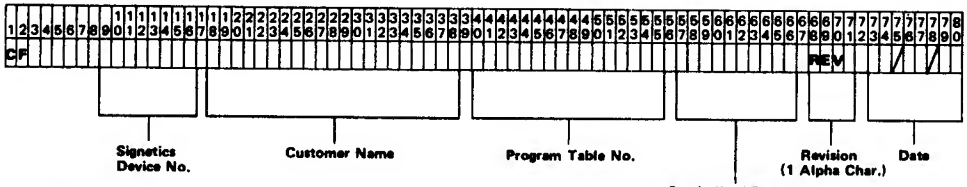
*Both input and output fields of unused P-terms can be left blank.

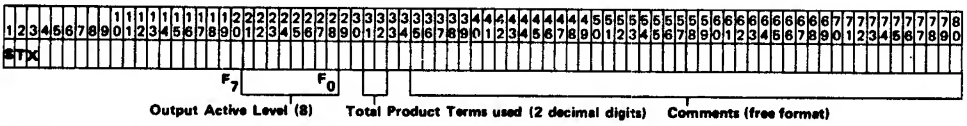
PUNCHED CARD CODING FORMAT

The FPLA Program Table can be supplied directly to Signetics in Punched Card form, using standard 80-column IBM cards. For each FPLA Program Table, the customer should prepare an input card deck in accordance with the following format:

CARD No. 1 - Free format within designated fields.



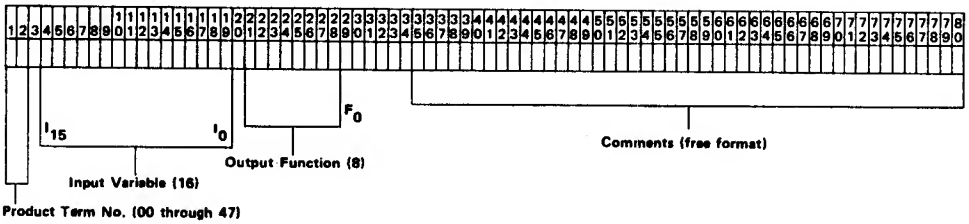
CARD No. 2 -



Output Active Level entries are determined in accordance with the following table:

OUTPUT ACTIVE LEVEL	
ACTIVE HIGH	ACTIVE LOW
H	L

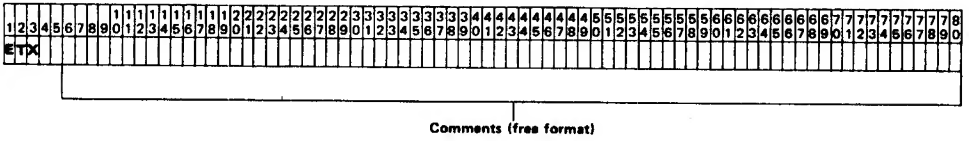
CARD No. 3 through No. 50



Input Variable and Output Function entries are determined in accordance with the following table:

INPUT VARIABLE			OUTPUT FUNCTION	
I_m	I_m	DON'T CARE	PROD. TERM PRESENT IN F_p	PROD. TERM NOT PRESENT IN F_p
H	L	X	A	–
Note: All unused inputs must be programmed as DON'T CARE.			*Note: Output Function entries are independent of programmed output polarity.*	

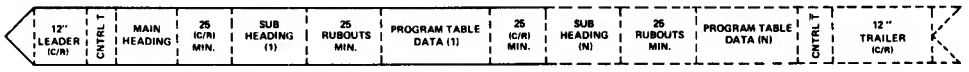
CARD No. 51



Note: Product Term cards 3 through 50 can be in any order. Not all 48 Product Terms need to be present. Unused Product Terms require no entry cards, and will be skipped during the actual programmin sequence.

PAPER TAPE CODING FORMAT

The FPLA Program Table can also be sent to Signetics in ASCII tape format via TWX, or air mail using any type of 8-level tape(paper, mylar, fanfold, etc.). A number* of Program Tables can be sequentially assembled on a continuous tape as follows:



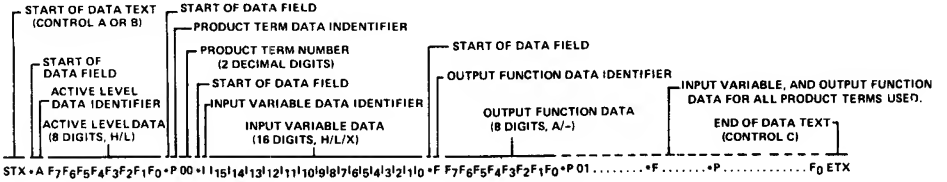
A. The MAIN HEADING at the beginning of tape includes the following information, with each entry preceded by a ($) character, whether used or not:

1. **Customer Name**_____
2. **Customer TWX No.**_____
3. **Date**_____
4. **Purchase Order No.** _____
5. **Number of Program Tables** _____
6. **Total Number of Parts** _____

B. Each SUB HEADING should contain specific information pertinent to each Program Table as follows, with each entry preceded by a ($) character, whether used or not:

1. **Signetics Device No.** _____
2. **Program Table No.** _____
3. **Revision** _____
4. **Date** _____
5. **Customer Symbolized Part No.** _____
6. **Number of Parts**_____

C. Program Table data blocks are initiated with an STX character, and terminated with an ETX character. The body of the data consists of Output Active Level, Product Term, and Output Function information seperated by appropriate identifiers in accordance with the following format:



Entries for the 3 Data Fields are determined in accordance with the following Table:

INPUT VARIABLE			OUTPUT FUNCTION		OUTPUT ACTIVE LEVEL	
I_m	I_m	DON'T CARE	PROD. TERM PRESENT, IN F_p	PROD. TERM NOT PRESENT IN F_p	ACTIVE HIGH	ACTIVE LOW
H	L	X	A	–	H	L
Note: All unused inputs must be programmed as DON'T CARE.			*Note: Output Function entries are independent of programmed output polarity*		*Note: Output Polarity programmed once only*	

Although the Product Term data are shown entred in sequence, this is not necessary. It is possible to input only one Product Term, if desired. Unused Product Terms require no entry. ETX signalling end of Program Table may occur with less than the maximum number of Product Terms entered.

Carriage returns, line feeds, and rubout statements may be interspersed between data groups to facilitate an orderly, easily readable teletype printout. This information will be ignored by the programmer during programming. Comments are also allowed between data fields, provided that an asterisk (*) is not used in any heading or comment entry. When correcting or deleting entries, limit consecutive rubouts to less than 25.

* *Limit tape length to a roll of 1.75 inch inside diameter, and 4.25 inch outside diameter.*